REMARKS

Claims 1-10 have been cancelled and new claims 11-34 have been added. Claims 11-34 are pending, with claim 11 being independent.

Copies of the following three references were submitted on August 8, 2000, when the present application was filed, together with a sheet entitled "List of the Prior Art References Cited in the Specification":

> Japanese references 9-74352 and 11-15541 (each including an English abstract)
>
> V. von Kaenel et al., "A 600MHz CMOS PLL Microprocessor Clock Generator with a 1.2GHz VCO", 1998 IEEE International Solid-State Circuits Conference Digest of Technical Papers, April 1998, pp. 396-397, ISBN 0-7803-4344-1 (paper presented on February 7, 1998).

The 1998 IEEE International Solid-State Circuits Conference Digest of Technical Papers is cited on page 1 of the specification.

Japanese reference 11-15541 is cited on page 2 of the specification.

Japanese reference 9-74352 is cited on page 26 of the specification.

Japanese references 9-74352 and 11-15541 are not in the English language.

The concise explanation of the relevance of Japanese references 9-74352 and 11-15541 required by 37 CFR 1.98(a)(3)(i) is provided by the English abstracts of these referenced, and by the discussion of these references in the specification as permitted by the last sentence of 37 CFR 1.98(a)(3)(i).

It is submitted that the Examiner was required by 37 CFR 1.97 and 1.98 and MPEP 609 to consider the three references discussed above in the first

Office Action of January 16, 2002. However, the Office Actions of January 16, 2002, and June 25, 2002, do not indicate that these three references have been considered.

Accordingly, it is respectfully requested that these three references be considered. Attached hereto is a form PTO-1449 listing these three references for the Examiner's convenience in indicating that these three references have been considered.

Claims 1-10 were rejected under 35 USC 103(a) as being unpatentable over Gersbach et al. (Gersbach) (U.S. Patent No. 5,485,126) in view of Atriss et al. (Atriss) (U.S. Patent No. 5,304,955). Although this rejection has been rendered moot by the cancellation of claims 1-10, the rejection is respectfully traversed insofar as it may be deemed to be applicable to new claims 11-34.

In explaining the rejection of claims 1-10 in the Office Action of June 25, 2002, the Examiner states as follows:

> Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gersbach et al.(of record, 5,485,126) and further in view of Atriss et al(US 5,304,955)
>
> The ring oscillator with three inverters, as disclosed by Gersbach et al, discloses use in a PLL with phase detector(see figure 3 for VCO). A first MOS(Q9), and first and second capacitors(Q17,18) are shown.
>
> The reference does not highlight the fact that PLL's also make use of frequency comparators that provide coarse tuning which then changes to fine tuning by way of the phase detection control. This is notoriously well known in the art. Also, a feedback divider or reference divider allows for specific frequency control as is conventional too in PLL

systems. The additive which control the frequency by **a digital signal**(1 bit at a time) is not shown.

With regards these ideas, the reference by Atriss et al discloses a PLL(integrated)(see figure 1), that makes use of all the notorious loop elements such as phase detector(14), frequency detector, VCO(22), and divider(30). Also shown is the additive control means(36,38) that allow for the digital control of the VCO output frequency in addition to the control input on transistor(150).

In light of the above it would have been recognized by one of ordinary skill in the art to have made use of the frequency comparison and divider elements in the broadly described PLL of Gersbach et al to generate a desired PLL synthesizer output as is notoriously well known in the art and as highlighted by Atriss et al including the additional digital control feature to further enhance the frequency output.

In explaining the rejection, the Examiner has not specifically referred to any of claims 1-10 in explaining the rejection, and has not specifically pointed out where many of the features recited in claims 1-10 are disclosed or suggested by Gersbach and Atriss, which makes it difficult for the applicants to respond to the rejection.

Accordingly, in the event the Examiner should reject any of new claims 11-34 over the prior art, it is respectfully requested that the Examiner specifically point out where each feature of each rejected claim is disclosed or suggested in the prior art.

Independent claim 11 recite a voltage controlled oscillator, comprising a first node connected to a first power source having a first voltage, a second node connected to a second power source having a second voltage, a first MOS transistor, an oscillator arranged between the first node and a third node, and a

first capacitive element arranged between the first node and the third node, wherein an oscillation frequency of the oscillator is controlled by connecting a source of the first MOS transistor to the second node, connecting a drain of the first MOS transistor to the third node, applying an analog control signal to a gate of the first MOS transistor, and changing a frequency of a high level and a low level of a digital control signal.

It is submitted that Gersbach and Atriss do not disclose or suggest the combination of features recited in claim 11 which are underlined above, particularly the feature of claim 11 wherein an oscillation frequency of the oscillator is controlled by connecting a source of the first MOS transistor to the second node, connecting a drain of the first MOS transistor to the third node, applying an analog control signal to a gate of the first MOS transistor, and changing a frequency of a high level and a low level of a digital control signal.

Although Fig. 4 of Atriss shows controlling a frequency of a voltage controlled oscillator 22 with digital control signals DL0-DL5, it is not seen where this is done by changing a frequency of a high level and a low level of digital control signals DL0-DL5 as would be required to provide the feature of claim 11 wherein an oscillation frequency of the oscillator is controlled by . . . changing a frequency of a high level and a low level of a digital control signal.

Dependent claim 12 recites a voltage controlled oscillator according to claim 11, further comprising a second capacitive element, and a node to the second capacitive element, wherein connection to and disconnection from the second capacitive element are selected according to the digital control signal.

It is submitted that Gersbach and Atriss do not disclose or suggest the features of claim 12 which are underlined above in combination with all of the features recited in claim 11 from which claim 12 depends.

Dependent claims 13, 21, and 28 recite a voltage controlled oscillator according to claims 12, 20, and 11, respectively, wherein the oscillator includes at least three inverters each formed by connecting a drain of a P-channel MOS transistor to a drain of an N-channel MOS transistor, and wherein the inverters are looped by sequentially connecting respective output terminals of the inverters to respective input terminals of the inverters.

It is submitted that Gersbach and Atriss do not disclose or suggest the features of claims 13, 21, and 28 which are underlined above in combination with all of the features recited in claims 12, 20, and 11 from which claims 13, 21, and 28 depend.

Dependent claims 14, 17, 22, 25, 29, and 32 recite a phase-locked loop (PLL) circuit, comprising a voltage controlled oscillator according to claims 13, 12, 21, 20, 28, and 11, respectively, a frequency divider, a phase comparator, a frequency comparator, and a control circuit, wherein the frequency divider outputs a divided output signal obtained by dividing a frequency of an output signal from the voltage controlled oscillator, wherein the phase comparator receives a reference signal and the divided output signal, compares a phase of the reference signal with a phase of the divided output signal, and outputs a phase difference detection signal, wherein the frequency comparator receives the reference signal and the divided output signal, compares a frequency of the

reference signal with a frequency of the divided output signal, and outputs a frequency difference detection signal, wherein the control circuit receives the phase difference detection signal and the frequency difference detection signal and outputs the analog control signal to execute control according to the phase difference detection signal and the frequency difference detection signal, and wherein the phase difference detection signal corresponds to the digital control signal.

It is submitted that Gersbach and Atriss do not disclose or suggest the features of claims 14, 17, 22, 25, 29, and 32 which are underlined above in combination with all of the features recited in claims 13, 12, 21, 20, 28, and 11 from which claims 14, 17, 22, 25, 29, and 32 depend.

Dependent claims 15, 23, and 30 recite a phase-locked loop (PLL) circuit according to claims 14, 22, and 29, respectively, wherein the control circuit also receives the reference signal, wherein the control circuit executes control according to the phase difference detection signal and the frequency difference detection signal every cycle of the reference signal, and wherein a variation of a voltage of the analog control signal according to the frequency difference detection signal is larger than a variation of the voltage of the analog control signal according to the phase difference detection signal.

It is submitted that Gersbach and Atriss do not disclose or suggest the features of claims 15, 23, and 30 which are underlined above in combination with all of the features recited in claims 14, 22, and 29 from which claims 15, 23, and 30 depend.

Dependent claims 16, 24, and 31 recite a phase-locked loop (PLL) circuit according to claims 14, 22, and 29, respectively, wherein the control circuit has a control cycle in which the control circuit executes control according to the phase difference detection signal and the frequency difference detection signal every cycle of the reference signal, and wherein the frequency comparator includes means for comparing the frequency of the reference signal with the frequency of the divided output signal, and means for preventing a variation of a voltage of the analog control signal according to the phase difference detection signal in a first control cycle in which the frequency difference detection signal corresponding to a detection of a frequency difference is outputted and in a predetermined number of control cycles following the first control cycle.

It is submitted that Gersbach and Atriss do not disclose or suggest the features of claims 16, 24, and 31 which are underlined above in combination with all of the features recited in claims 14, 22, and 29 from which claims 16, 24, and 31 depend.

Dependent claims 18, 26, and 33 recite a phase-locked loop (PLL) circuit according to claims 17, 25, and 32, respectively, wherein the control circuit also receives the reference signal, wherein the control circuit executes control according to the phase difference detection signal and the frequency difference detection signal every cycle corresponding to one cycle of the reference signal, and wherein a variation of a voltage of the analog control signal according to the frequency difference detection signal is larger than a variation of the voltage of the analog control signal according to the phase difference detection signal.

It is submitted that Gersbach and Atriss do not disclose or suggest the features of claims 18, 26, and 33 which are underlined above in combination with all of the features recited in claims 17, 25, and 32 from which claims 18, 26, and 33 depend.

Dependent claims 19, 27, and 34 recite a phase-locked loop (PLL) circuit according to claims 17, 25, and 32, respectively, wherein the control circuit has a control cycle in which the control circuit executes control according to the phase difference detection signal and the frequency difference detection signal every cycle of the reference signal, and wherein the frequency comparator includes means for comparing the frequency of the reference signal with the frequency of the divided output signal, and means for preventing a variation of a voltage of the analog control signal according to the phase difference detection signal in a first control cycle in which the frequency difference detection signal corresponding to a detection of a frequency difference is outputted and in a predetermined number of control cycles following the first control cycle.

It is submitted that Gersbach and Atriss do not disclose or suggest the features of claims 19, 27, and 34 which are underlined above in combination with all of the features recited in claims 17, 25, and 32 from which claims 19, 27, and 34 depend.

Dependent claim 20 recites a voltage controlled oscillator according to claim 11, further comprising a third capacitive element, and a second MOS transistor, wherein the second MOS transistor is used for a switch to the third capacitive element, and wherein connection to and disconnection from the third

capacitive element are selected by inputting the digital control signal to a gate of the second MOS transistor.

It is submitted that Gersbach and Atriss do not disclose or suggest the features of claim 20 which are underlined above in combination with all of the features recited in claim 11 from which claim 20 depends.

Since Gersbach and Atriss do not disclose or suggest the features of claims 11-34 discussed above, it is submitted that claims 11-34 patentably distinguish over Gersbach and Atriss references in the sense of 35 USC 103(a), and an indication to that effect is respectfully requested.

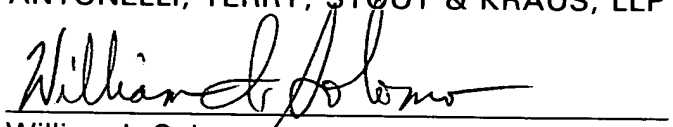
It is submitted that the Examiner's only rejection has been overcome, and that the application is now in condition for allowance. Reconsideration of the application and an action of a favorable nature are respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any

overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (520.38856X00).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



William I. Solomon
Registration No. 28,565

MK/WIS/RSS
(703) 312-6600

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